FIGURE 1

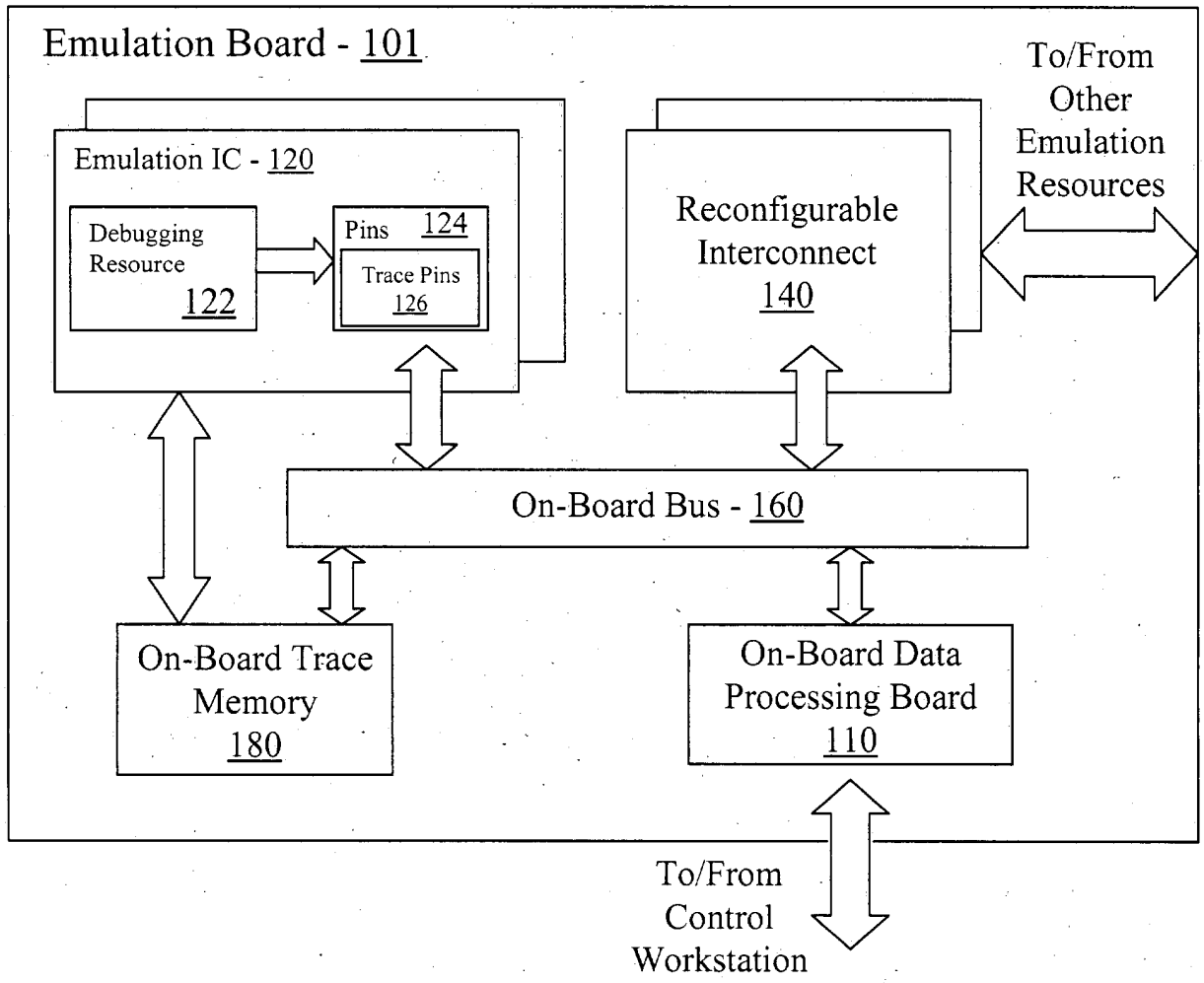

Emulation Board - 101
Emulation IC - 120
Debugging Resource 122
Pins 124
Trace Pins 126
Reconfigurable Interconnect 140
To/From Other Emulation Resources
On-Board Bus - 160
On-Board Trace Memory 180
On-Board Data Processing Board 110
To/From Control Workstation

FIGURE 2

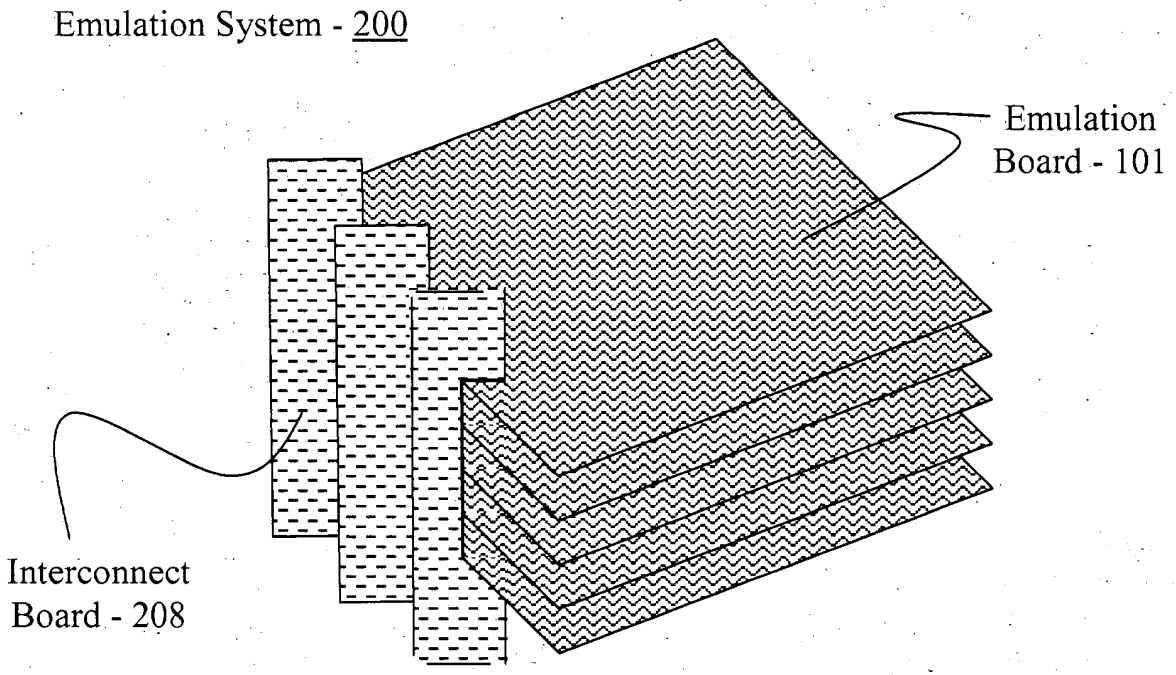

Emulation System - 200
Emulation Board - 101
Interconnect Board - 208

FIGURE 3

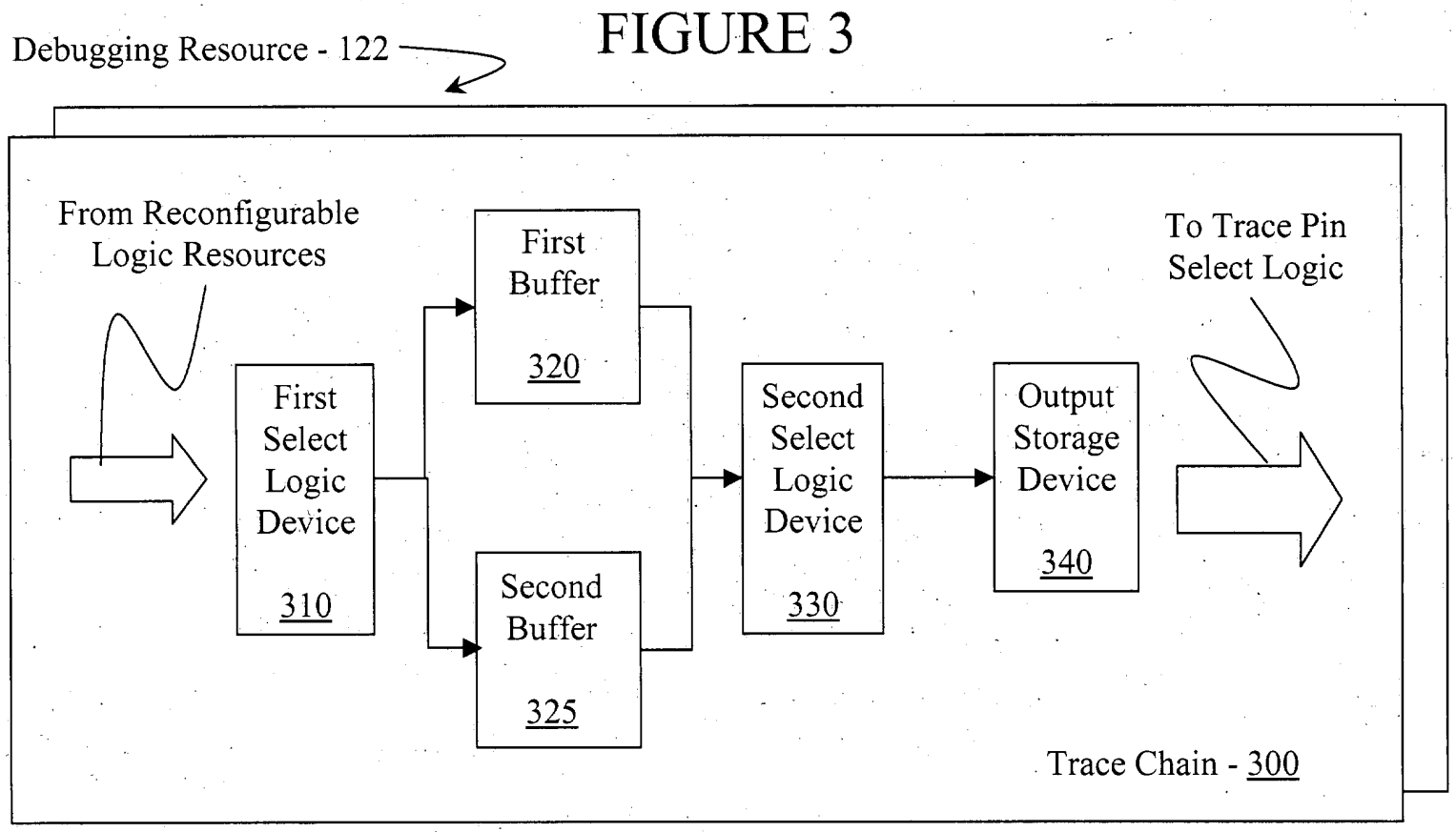

Debugging Resource - 122
From Reconfigurable Logic Resources
First Select Logic Device 310
First Buffer 320
Second Buffer 325
Second Select Logic Device 330
Output Storage Device 340
To Trace Pin Select Logic
Trace Chain - 300

FIGURE 4A

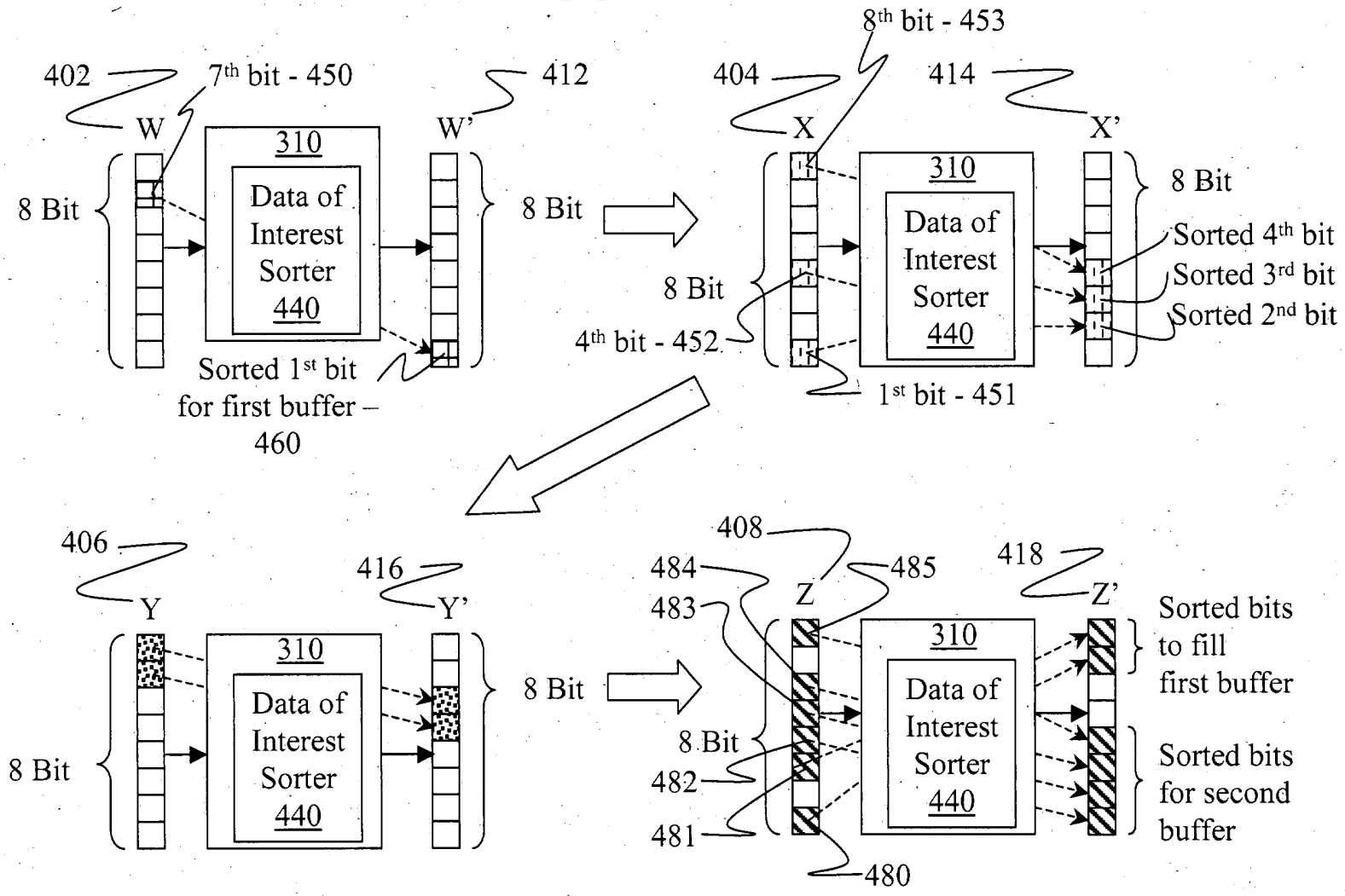
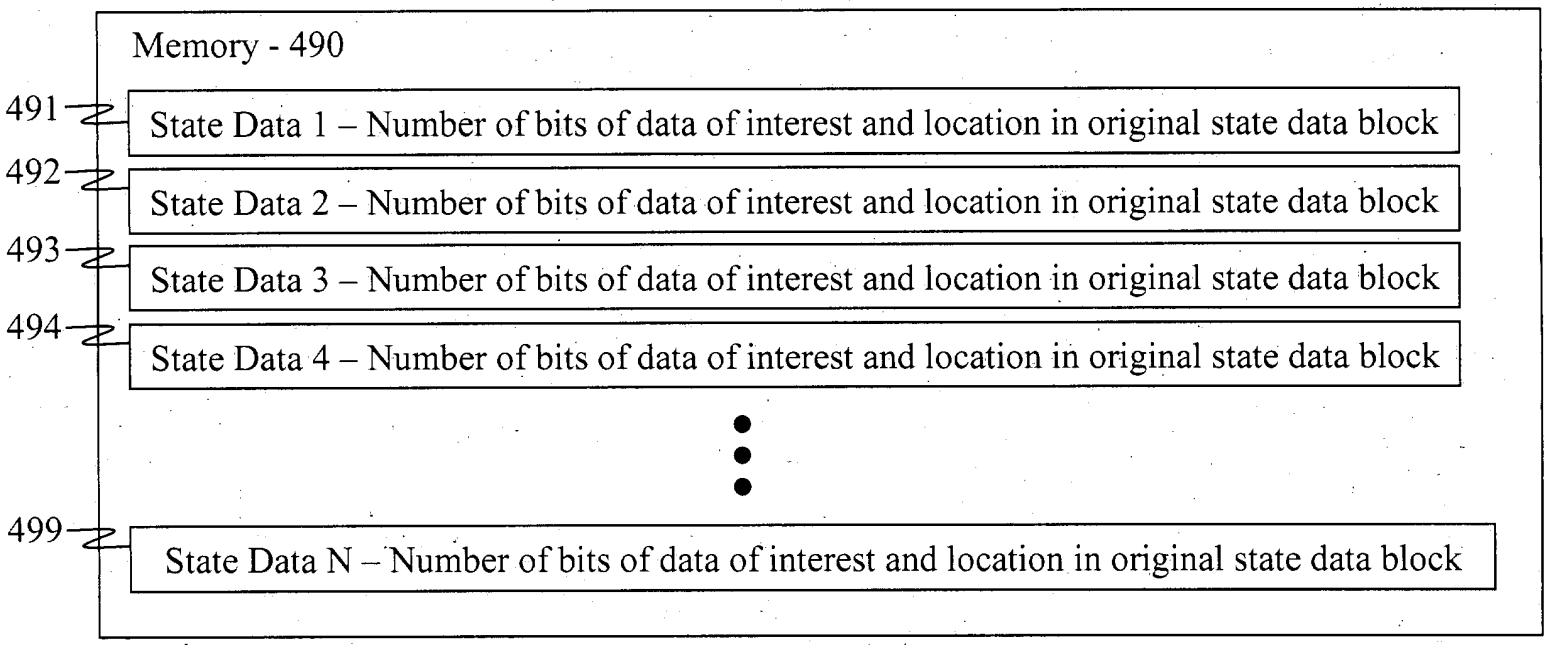

402
7th bit - 450
412
W
W'
310
Data of Interest Sorter 440
8 Bit
8 Bit
Sorted 1st bit for first buffer – 460
8th bit - 453
404
414
X
X'
310
Data of Interest Sorter 440
8 Bit
Sorted 4th bit
Sorted 3rd bit
Sorted 2nd bit
8 Bit
4th bit - 452
1st bit - 451
406
416
Y
Y'
310
Data of Interest Sorter 440
8 Bit
8 Bit
408
484
485
418
483
Z
Z'
310
Data of Interest Sorter 440
Sorted bits to fill first buffer
Sorted bits for second buffer
8 Bit
482
481
480

FIGURE 4B


Memory - 490
491
State Data 1 – Number of bits of data of interest and location in original state data block
492
State Data 2 – Number of bits of data of interest and location in original state data block
493
State Data 3 – Number of bits of data of interest and location in original state data block
494
State Data 4 – Number of bits of data of interest and location in original state data block
499
State Data N – Number of bits of data of interest and location in original state data block

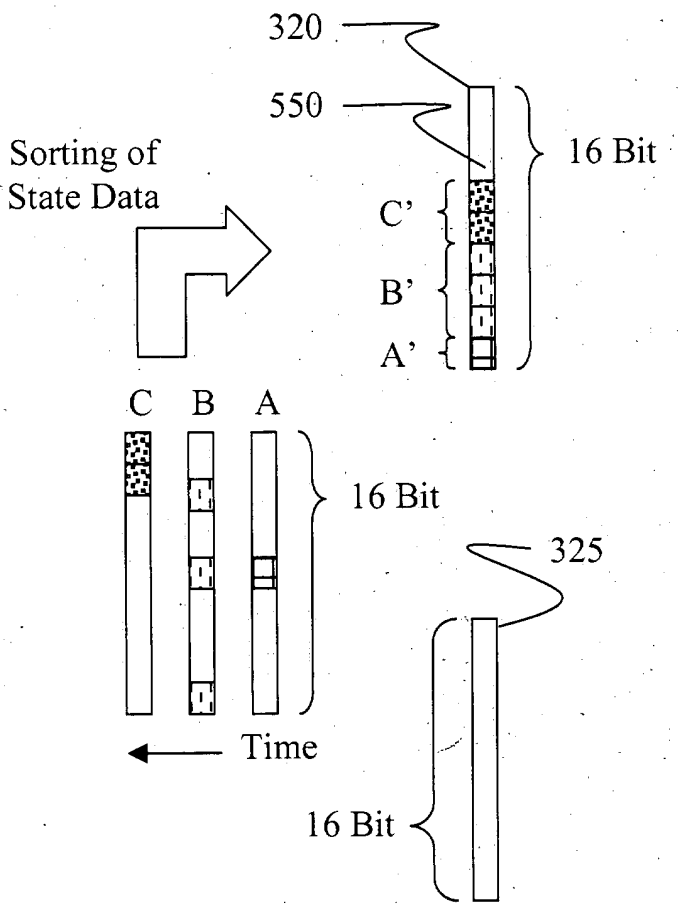


FIGURE 5A

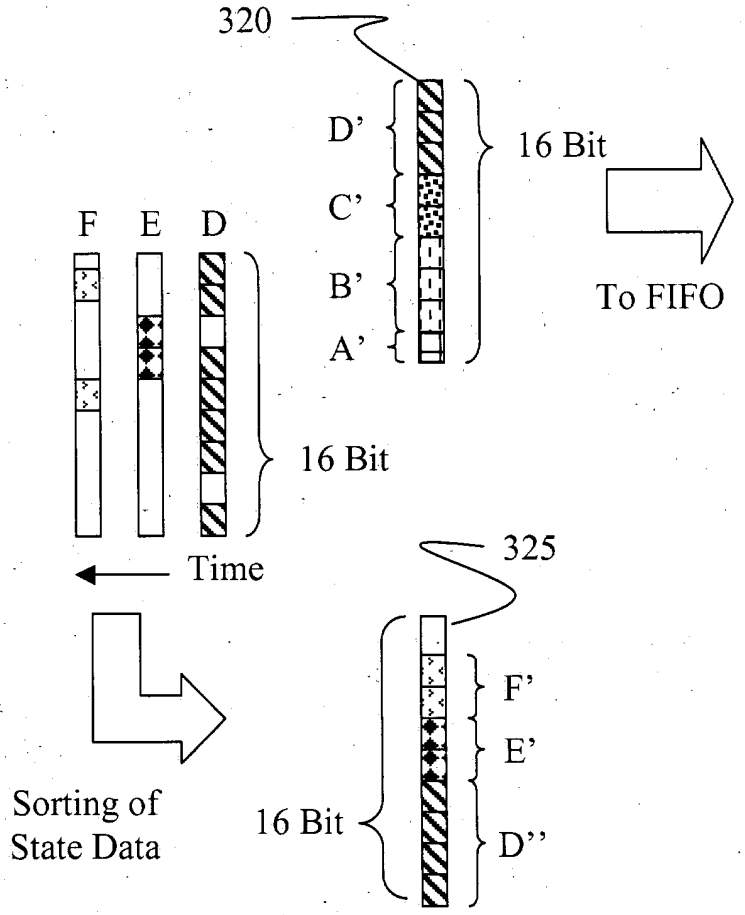


FIGURE 5B

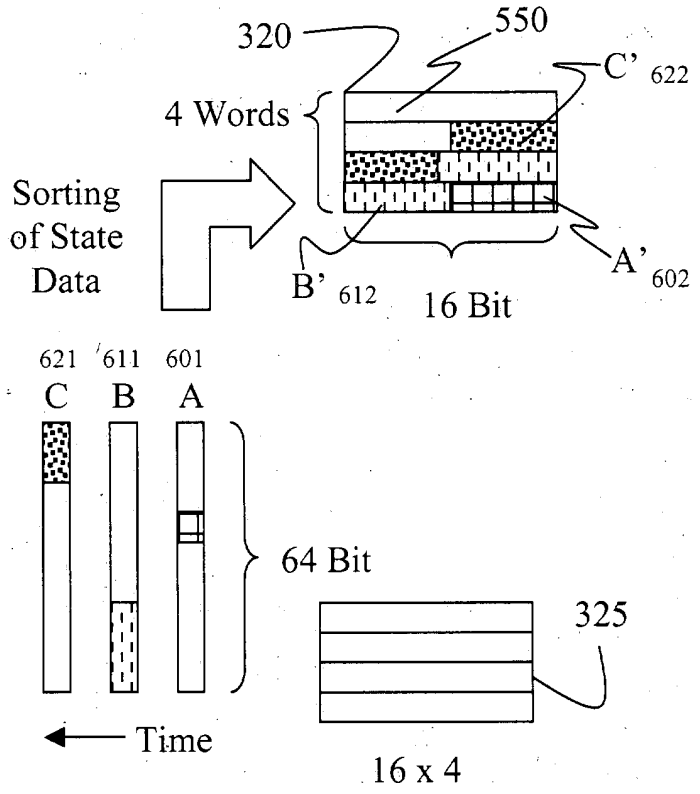


FIGURE 6A

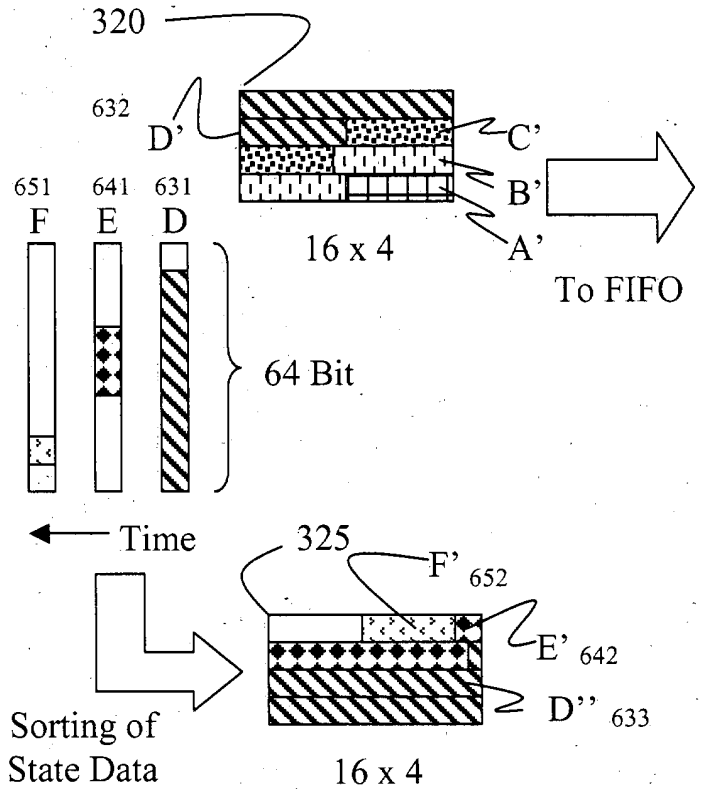
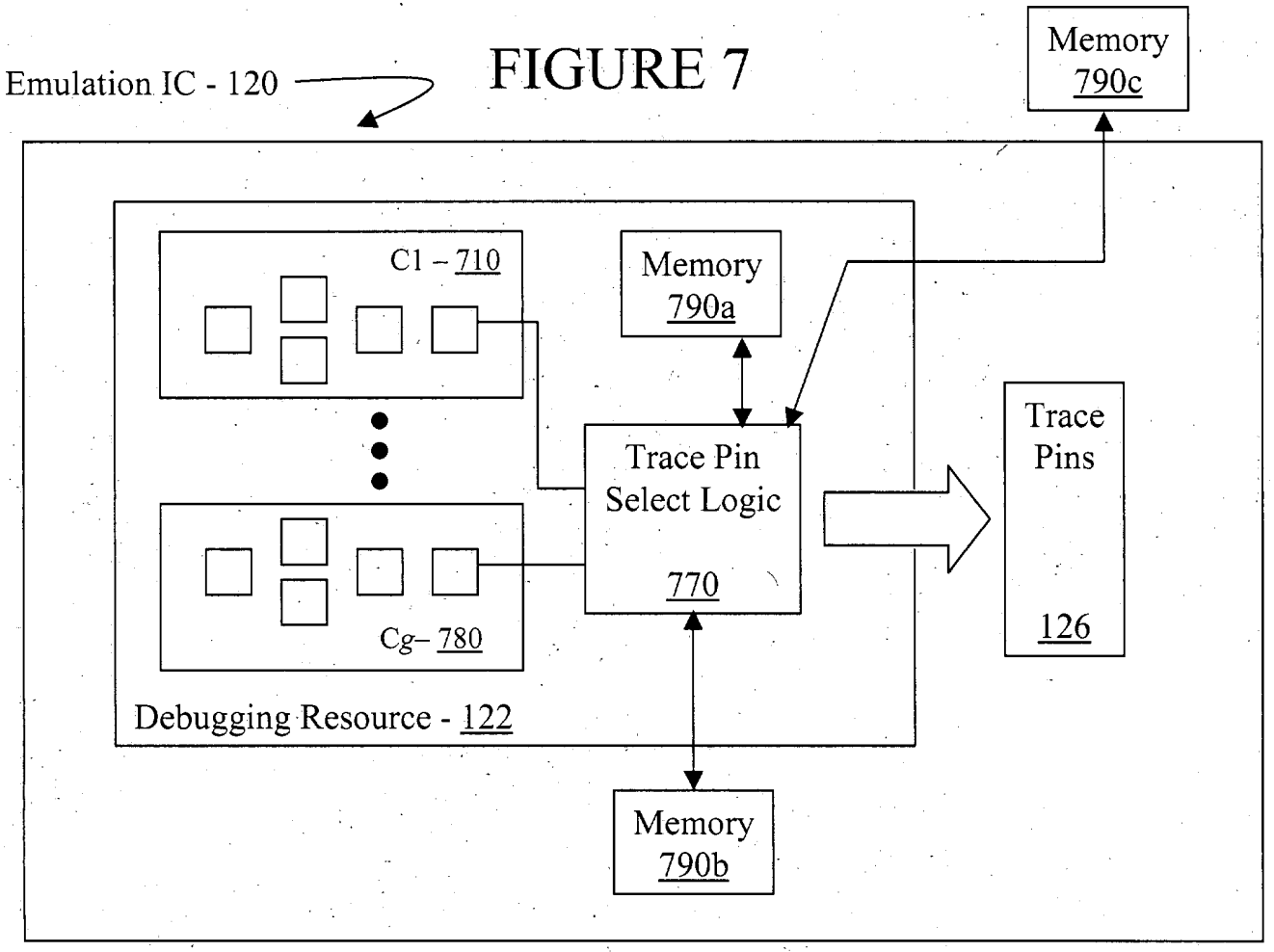


FIGURE 6B

FIGURE 7


Emulation IC - 120
Memory
790c
C1 – 710
Memory
790a
Trace Pin
Select Logic
770
Trace
Pins
126
Cg– 780
Debugging Resource - 122
Memory
790b

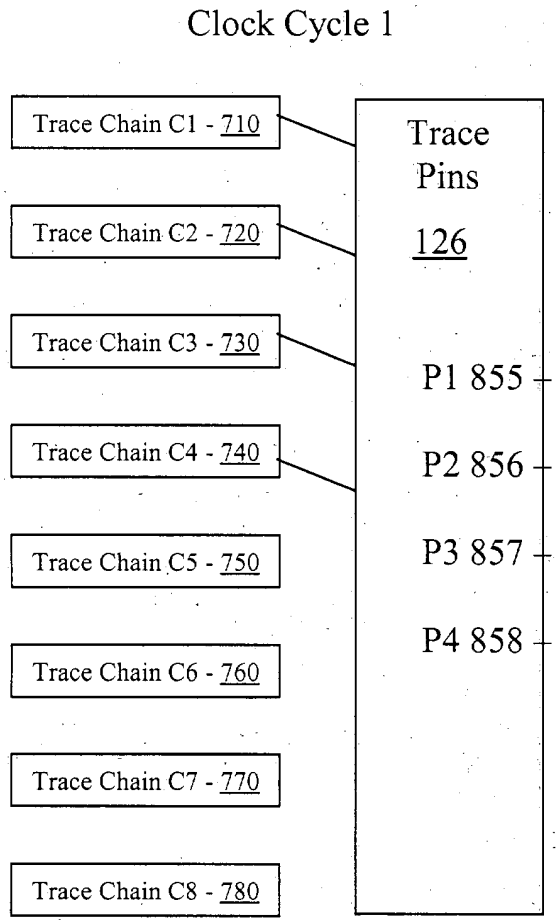


FIGURE 8A

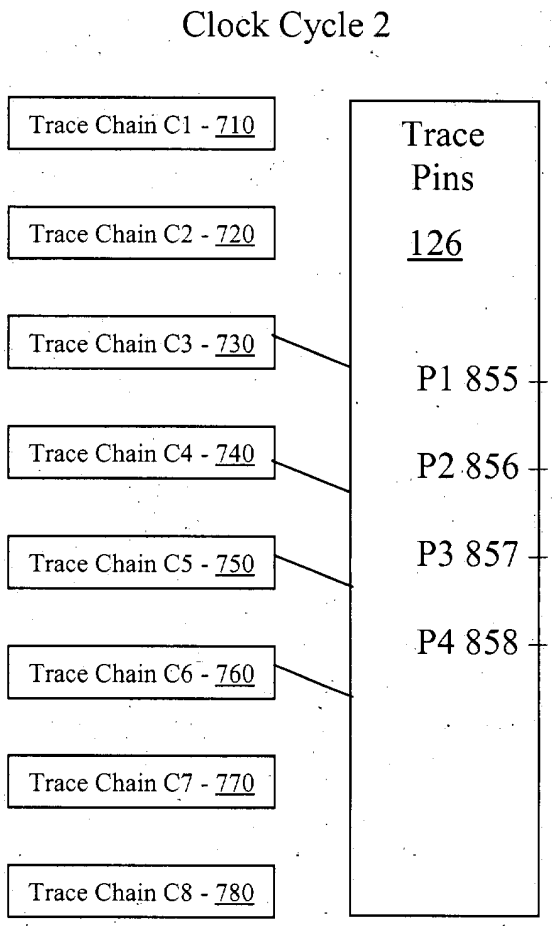


FIGURE 8B

Clock Cycle 3

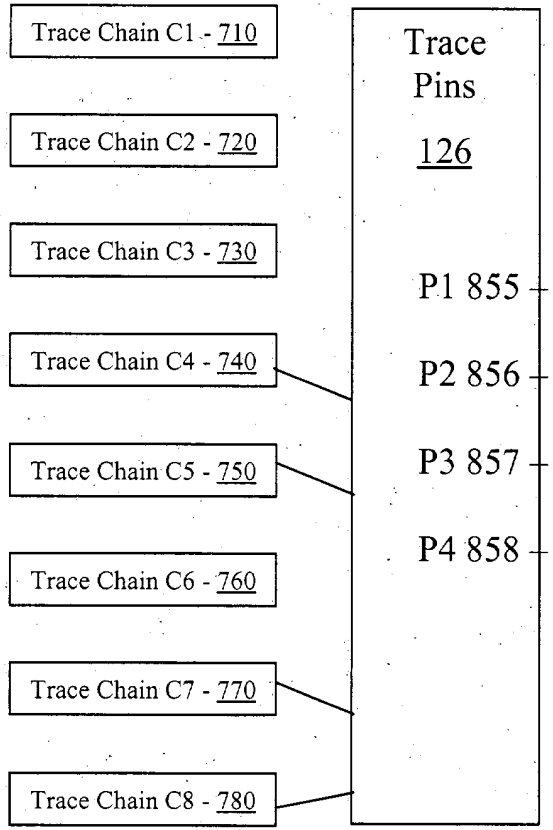


FIGURE 8C

FIGURE 9A

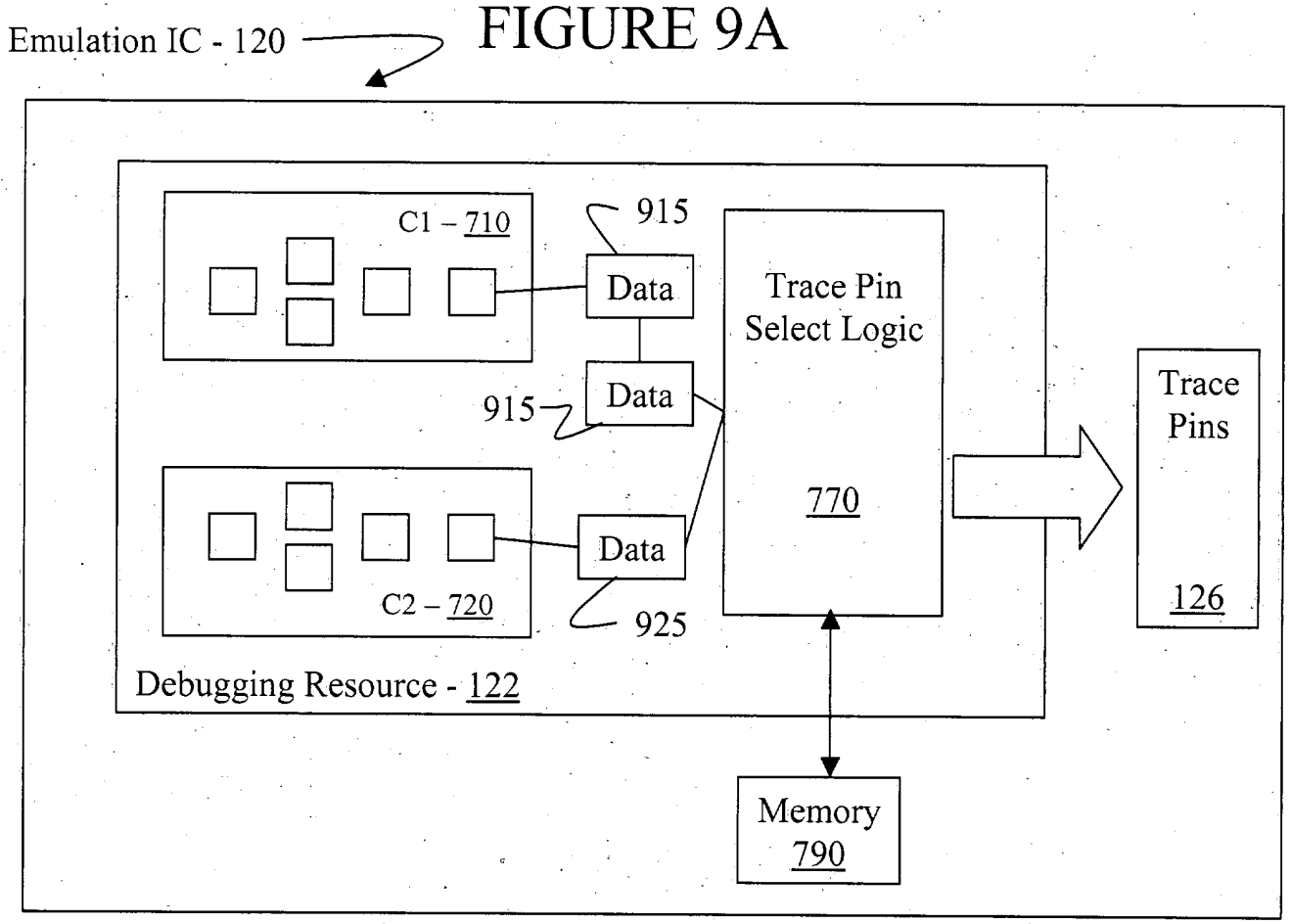

Emulation IC - 120
C1 – 710
915
Data
Trace Pin
Select Logic
915
Data
770
Trace
Pins
126
Data
C2 – 720
925
Debugging Resource - 122
Memory
790

FIGURE 9B

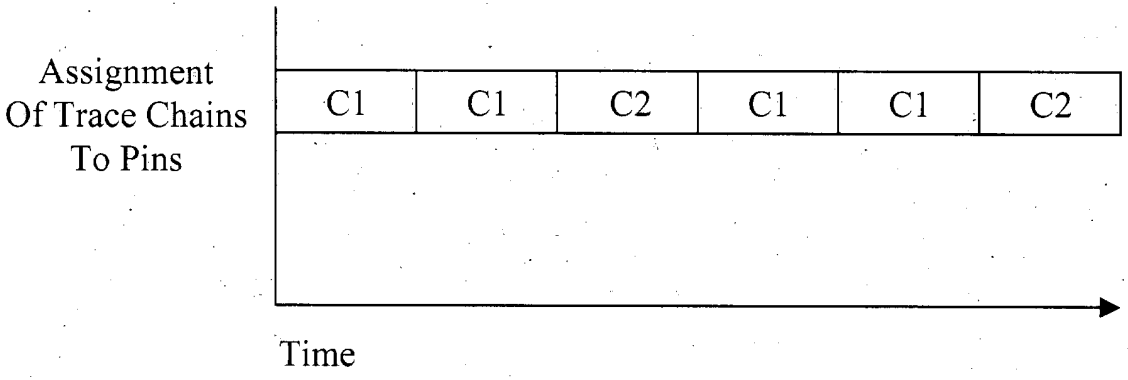


FIGURE 10

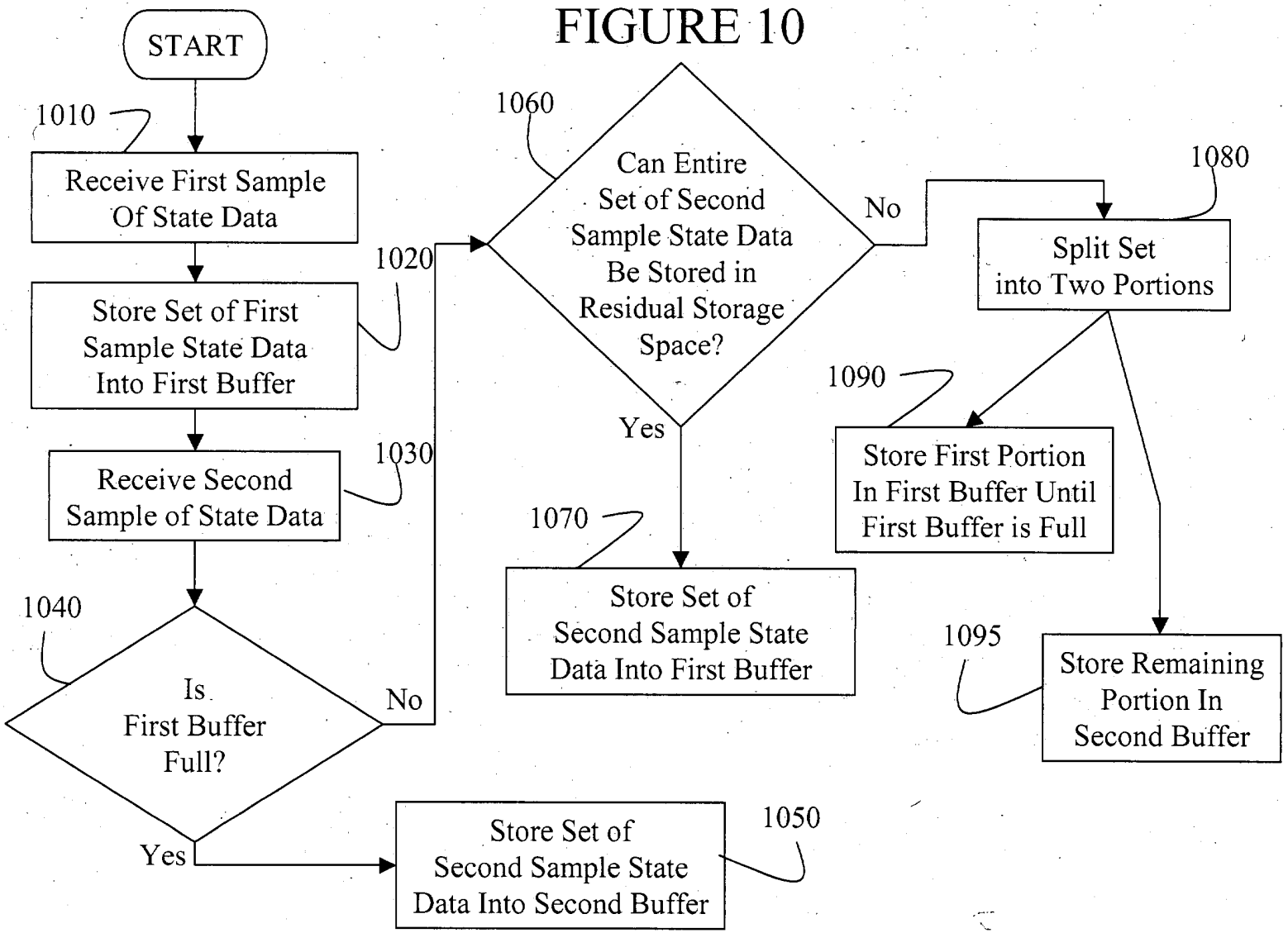
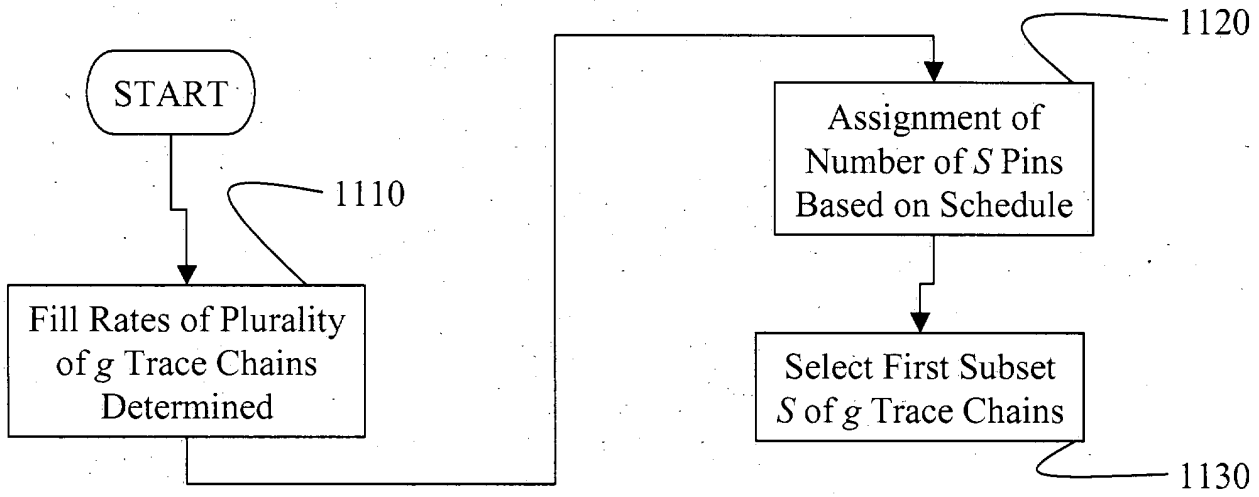

START
1010
Receive First Sample Of State Data
1020
Store Set of First Sample State Data Into First Buffer
1030
Receive Second Sample of State Data
1040
Is First Buffer Full?
No
Yes
1050
Store Set of Second Sample State Data Into Second Buffer
1060
Can Entire Set of Second Sample State Data Be Stored in Residual Storage Space?
Yes
1070
Store Set of Second Sample State Data Into First Buffer
No
1080
Split Set into Two Portions
1090
Store First Portion In First Buffer Until First Buffer is Full
1095
Store Remaining Portion In Second Buffer

FIGURE 11


START
1110
Fill Rates of Plurality of g Trace Chains Determined
1120
Assignment of Number of S Pins Based on Schedule
Select First Subset S of g Trace Chains
1130